

WEST Search History

DATE: Friday, September 16, 2005

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		<i>DB=PGPB; PLUR=YES; OP=ADJ</i>	
<input type="checkbox"/>	L31	(peripheral device and dynamically mapping and dynamically unmappable).clm.	0
<input type="checkbox"/>	L30	(peripheral device and dynamically mapping and dynamically unmappable).clms.	0
<input type="checkbox"/>	L29	(peripheral device and first request and second request and dynamically mapping and dynamically unmappable).clms.	0
		<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>	
<input type="checkbox"/>	L28	((mark and einkauf) or (herbert and ledebohm) or (franck and diard) or (jeffrey and doughty)).in.	34
<input type="checkbox"/>	L27	l24 not l26	168
<input type="checkbox"/>	L26	l22 and l23	3
<input type="checkbox"/>	L25	l22 and l24	0
<input type="checkbox"/>	L24	l21 not (l22 or L23)	168
<input type="checkbox"/>	L23	L21 and peripheral	39
<input type="checkbox"/>	L22	L21 and (demap\$5 or de-map\$5 or un-map\$5 or unmap\$5)	21
<input type="checkbox"/>	L21	l18 not l20	225
<input type="checkbox"/>	L20	L18 and (coprocessor or co-processor or co processor)	2
<input type="checkbox"/>	L19	L18 and l12	227
<input type="checkbox"/>	L18	L17 and l5	227
<input type="checkbox"/>	L17	L16 and l3	349
<input type="checkbox"/>	L16	((demap\$5 or de-map\$5 or un-map\$5 or unmap\$5 or deallocat\$4 or de-allocat\$ or unallocat\$4 or un-allocat\$ or remov\$ or delet\$5 or eliminat\$) ADJ3 (map or maps or translation table or TLB or (translation near2 index\$4))).ab,ti,bsum.	599
<input type="checkbox"/>	L15	l13 and L14	291
<input type="checkbox"/>	L14	((unmap\$5 or deallocat\$4 or de-allocat\$ or unallocat\$4 or un-allocat\$ or remov\$ or delet\$5 or eliminat\$) ADJ3 (map or maps or translation table or TLB or (translation near2 index\$4))).ab,ti,bsum.	576
<input type="checkbox"/>	L13	l9 and L12	585
<input type="checkbox"/>	L12	(map or maps or mapping or mapped or translation or tlb).ab,ti,bsum.	277907
<input type="checkbox"/>	L11	l9 and L10	583
<input type="checkbox"/>	L10	(map or maps or mapping or mapped or translation).ab,ti,bsum.	277275
<input type="checkbox"/>	L9	l4 and L8	2524

<input type="checkbox"/>	L8	((unmap\$5 or deallocat\$4 or de-allocat\$ or unallocat\$4 or un-allocat\$ or remov\$ or delet\$5 or eliminat\$) ADJ3 (map or maps or table or index)).ab,ti,bsum.	6692
<input type="checkbox"/>	L7	l4 and L6	13115
<input type="checkbox"/>	L6	l4 or L5	1665701
<input type="checkbox"/>	L5	(cpu or processor or coprocessor or microprocessor or host)	1661183
<input type="checkbox"/>	L4	l2 and L3	13115
<input type="checkbox"/>	L3	(memory or memories or storage)	3445839
<input type="checkbox"/>	L2	(unmap\$5 or deallocat\$4 or de-allocat\$ or unallocat\$4 or un-allocat\$ or remov\$ or delet\$5 or eliminat\$) ADJ3 (map or maps or table or index)	26305
		<i>DB=USPT; PLUR=YES; OP=ADJ</i>	
<input type="checkbox"/>	L1	6675262.pn.	1

END OF SEARCH HISTORY



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Virtual-Address Caches Part 1: Problems and Solutions in Uniprocessors

Michel Cekleov
Michel Dubois

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<http://doi.ieeecomputersociety.org/10.1109/40.621215>

Abstract

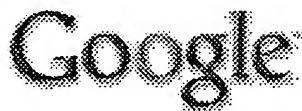
In order to support virtual memory, virtual addresses must be efficiently translated into physical addresses. Traditionally, this dynamic translation has been done in a Translation Lookaside Buffer (TLB) before or in parallel with the cache access, so that the cache is indexed and tagged with physical addresses. However, physical-address caches are either slow or limited in size. To solve this bottleneck, caches can be accessed directly with virtual addresses. Unfortunately, consistency problems add complexity to virtual-address caches. These problems are mostly caused by synonyms and address-mapping changes. In this first part, we

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introduce the problems and discuss solutions in the context of single-processor systems. In Part 2 of this two-part series, we will address multiprocessor issues.

 **References** [About References](#) | [Back to Top](#)

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